What is claimed is:

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1. A thin film transistor, comprising:

a stepped substrate provided with a sidewall between upper and lower portions thereof;

an active layer formed on the stepped substrate;

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a gate insulation film formed on the active layer;

a gate electrode formed on the gate insulation film corresponding to the sidewall of the substrate;

an insulation film formed on the gate insulation film between the gate electrode and the lower portion of the substrate; and

impurity regions in the active layer corresponding to the upper and lower portions of the substrate.

2. The thin film transistor of claim 1, wherein the stepped substrate is formed of an insulating material.

3. The thin film transistor of ~~claim~~ 1, wherein the insulation film is formed on the [upper] and lower portions, and ~~on the~~ sidewall of the substrate.

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4. The thin film transistor of claim 1, wherein the active layer is a semiconductor film.

5. ~~The thin film transistor of claim 1, wherein the~~ [insulation] ~~film is an SOG~~ insulating (spin-on-glass).

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6. The thin film transistor of claim 1, wherein a portion of the active layer corresponding to the gate electrode is a channel region, and a portion thereof corresponding to the insulation film is an offset region.

7. A method of fabricating a thin film transistor, comprising the steps of:

etching and patterning a substrate in order to form a sidewall between upper and lower portions thereof;

forming an active layer on the substrate;

forming a gate insulation film on the active layer;

forming an insulation film on a first region of the sidewall and on the lower portion of the substrate, and forming a gate electrode on a second region of the sidewall and on the insulation film; and

forming impurity regions in the active layer corresponding to the upper and lower portions of the substrate.

8. The method of claim 7, wherein the substrate is an insulating material.

9. The method of claim 7, wherein the insulation film is formed on the upper and lower portions, and on the sidewall of the substrate.

10. The method of claim 7, wherein the active layer is a semiconductor film.

11. The method of claim 7, wherein the insulation film is an SOG (spin-on-glass).

12. The method of claim 7, wherein a portion of the active layer corresponding to the gate electrode is a channel region, and a portion thereof corresponding to the insulation film is an offset region.

13. The method of claim 7, wherein the step of forming the gate electrode and insulation film comprises the sub-steps of:

forming the insulation film on the lower portion of the substrate;

forming a conductive film on the upper portion and on the sidewall of the substrate, and on the insulation film;

forming a conductive sidewall on the sidewall of the substrate by applying an anisotropic etching process to the conductive film; and

etching the insulation film by using the conductive side wall as an etching mask.

14. The method of claim 13, wherein the conductive film is a polysilicon layer.